Full wave Analysis of Isolated Pockets to Improve Isolation performances in Silicon based Technology.

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Abstract — **This paper presents a versatile full wave analysis tool in which isolation pockets in IC's are readily introduced to perform intensive EM simulation including efficient introduction of via interconnects through metal levels. Obtained results are favorably compared to recent experimental published results.**

I. INTRODUCTION

To face the necessity of improving isolation capabilities of systems sensitive blocks, with the constant increase of the microprocessors frequency clock, investigations of Mixed Signal IC's designers lead to new isolation pattern configurations. Among the recently proposed substrate isolation patterns, Isolation Pockets have demonstrated significant improvement of pad to pad isolation performances as experimentally verified in [1]. Authors of [1], to describe silicon substrate coupling effects proposed an analysis based on RC network models. Thus, to find out the equivalent circuit model parameters, an extraction technique consisting of equating the measured S-parameters-data and analytical derived expressions is considered. Such extraction to be performed, intensive measurements with different resistivity ranges are required (5~8 Ω.cm, 25~50 Ω.cm and 2k Ω.cm). On the other hand, although RC network models allow the electrical representation of the investigated structure to be estimated, they find difficult ways to account for electromagnetic couplings between guard-rings and between guard-ring and pads connections, since CAD modeling of through via consider via as an isolated element even when constituting via fence or guard rings. Guard-rings constituting isolated pocket can be considered as via fence as presented in [2-4]. To account for disturbing EM couplings of different nature, EM analysis is inescapable [5-8] for an accurate full wave modeling exempting intensive measurements.

In this paper, we propose the investigation of pad to pad isolation capabilities in standard CMOS integrated circuits in presence of isolated pockets (IP), from an original full wave analysis saving considerable computational effort. The isolated pockets are accurately modeled using a simple and efficient EM approach in the spatial domain.

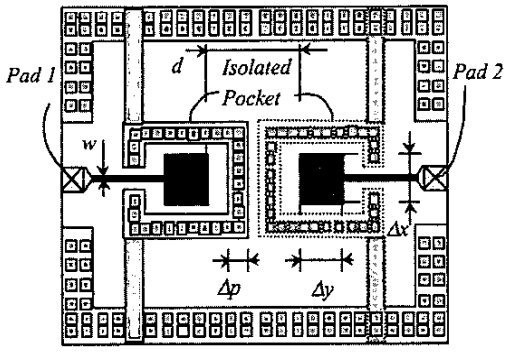
II. FULLWAVE ANALYSIS

A wave approach for multilayer circuits.

Let us consider for the beginning the combinations of tangential fields relatively to a surface X given by

$$\begin{vmatrix} A_{i,n}^{X} \\ B_{i,n}^{X} \end{vmatrix} = \frac{1}{2\sqrt{Z_r}} \begin{vmatrix} 1 & Z_r \\ 1 & -Z_r \end{vmatrix} \begin{vmatrix} E_{i,n}^{X} \\ J_{i,n}^{X} \end{vmatrix} \qquad (1)$$

in which Z_r is a reference wave impedance, $J_i = H_i \wedge n_i$



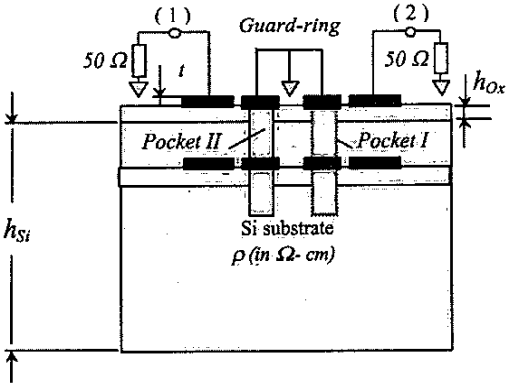


Fig.1. Structure pattern layout with one or two Isolated Pockets (a) – Cross-section of the structure with different metallization levels (b) - h_{Si}=220 μm, h_{Ox}=0.95 μm – t=0.8 μm.

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n_i being the outgoing normal on side i=1,2 with $u = x,y$. Although the "waves" defined in (1) are tangential vectors, it will be seen convenient later on to consider A and B in (1) as incoming (incident) and outgoing (reflected) waves relatively to the considered surface. From this point, the starting notice is that any kind of boundary condition impressed on the surface of a printed circuit by its patterns admits a transfer representation :

$$\begin{vmatrix} B^X_{1,u} \\ B^X_{2,u} \end{vmatrix} = \hat{S}^X \begin{vmatrix} A^X_{1,u} \\ A^X_{2,u} \end{vmatrix} \qquad (2)$$

Hence, multilevel circuits result in relationships such as :

$$\begin{vmatrix} B^X_{i,u} \\ B^Y_{i,u} \end{vmatrix} = \begin{vmatrix} \hat{S}^X & \hat{C}^{X-Y} \\ \hat{C}^{Y-X} & \hat{S}^Y \end{vmatrix} \begin{vmatrix} A^X_{i,u} \\ A^Y_{i,u} \end{vmatrix} \qquad (3)$$

between tangential fields in which $\hat{C}^{X-Y}$ represents the local coupling between parts of circuits in levels X and Y as for instance in presence of via interconnects.

Fullwave analysis.

In each homogenous layer between printed circuits, tangential fields are linked by integral relations derived from Green equations. Then, at each stage of a multilayered structure, tangential fields satisfy both, conditions on the surface according to the metallic and interconnect pattern and, integral relations. Standard integral formulations rely on the substitution of the first type of conditions into the later one which provides the integral equation and the subsequent integral operator to invert during the resolution. Nevertheless, from the definition of the waves in (1), the integral equation can emerge broken down into two parts following the block diagram in Fig 2 which suggests an iterative resolution procedure.

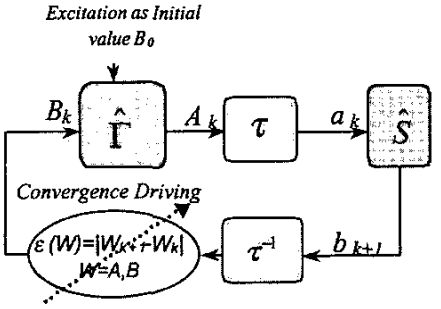

Fig. 2 Block diagram of the integral equation in terms of waves.

From the operators in Fig.2, the standard integral formulation states the solution as $A = \left(\hat{I} - \hat{\Gamma}\hat{S}\right)^{-1} B_0$, $\hat{I}$ and $\hat{\Gamma}$ being respectively the identity and Green operators. τ and τ^{-1} are unitary transforms allowing the calculation to be performed in the spatial and/or spectral domain, as convenient, and the convergence driving condition considers the response to the excitation source B_0 which acts as initial solution for the iterative resolution scheme.

Via-Hole Modeling.

Metal strips impose to the components of the tangential electric fields the condition :

$$E^X_{i,u} = 0 \qquad (4)$$

what ever the side i of the considered strip X and for both components $u = \perp, //$ respectively directed, in reference to the strip direction, in the perpandicular and longitudinal directions. The via connection between the two strips in Fig.3 impresses, to the longitudinal tangential components in the place of the via, instead of (4), the conditions :

$$(a)\ E^I_{2,//} = -E^{II}_{1,//} \quad and \quad (b)\ \begin{cases} J^I_{1,//} = J^{II}_{1,//} \\ J^I_{2,//} = J^{II}_{2,//} \end{cases} \qquad (5)$$

which express, due to the really short length of the via, a neglectible phase displacement accross the via (5-a) while condition (5-b) traduces the transposition of the magnetic field distribution from strip I to strip II and preserves the conservation of the current density.

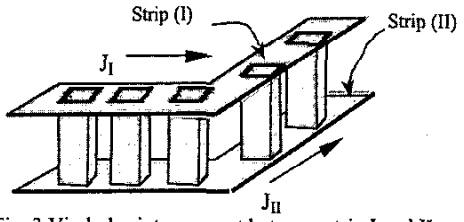

Fig. 3 Via-holes interconnect between strip I and II

In terms of waves, the above conditions introduced in (3) give, with $\eta(u) = \begin{cases} 1 \ if\ u = // \\ 0 \ if\ u = \perp \end{cases}$,

$$\hat{C}^{Y-X}\Big|_{\_} = (1+\alpha_{12}^2)^{-1} \begin{vmatrix} \alpha_{12}^2 - 1 & -2\alpha_{12}^2 \\ 2\alpha_{12}^2 & 1-\alpha_{12}^2 \end{vmatrix} \ with\ \alpha_{12} = \eta(u)\sqrt{Z_2/Z_1} \qquad (6)$$

Via crossing from metal M_i to metal M_{i+1}, in Fig.1, out-diagonal blocks in (3) are built step by step following (6). In this way, interconnect description does not introduce any additional expense in computation time

III. SIMULATION RESULTS

Inscrtion and isolation between pads in Fig.1 are presented in Fig.4 against frequency for different spacing d. The isolation decreasing as frequency grows, 15 dB shift is observed, all over the frequency range, between the 10 and 70 µm separation cases. Fig 5-a demonstrates an effectiveness around 10 dB in the upper part of the frequency band for an isolation pocket designed, as in [1], between M1 and the resistive substrate.

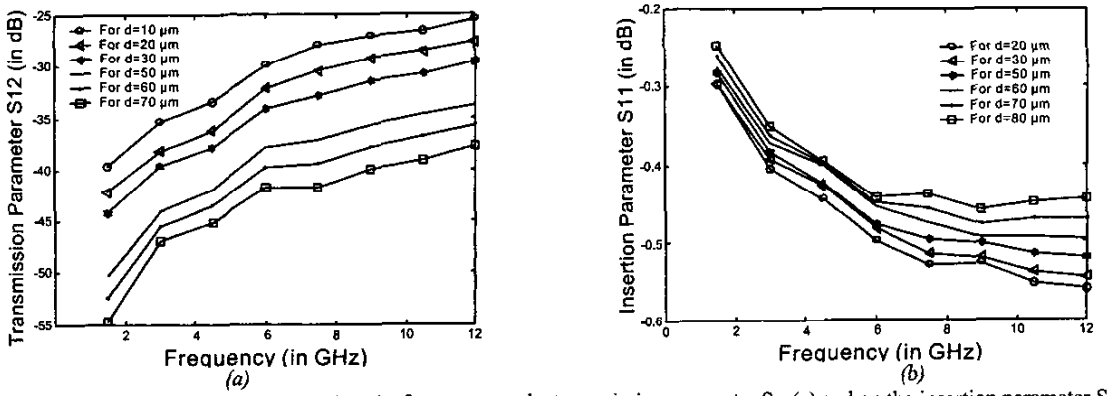

Fig.4 Influence of the pad spacing against the frequency on the transmission parameter S_{12} (a) and on the insertion parameter S_{11} (b).

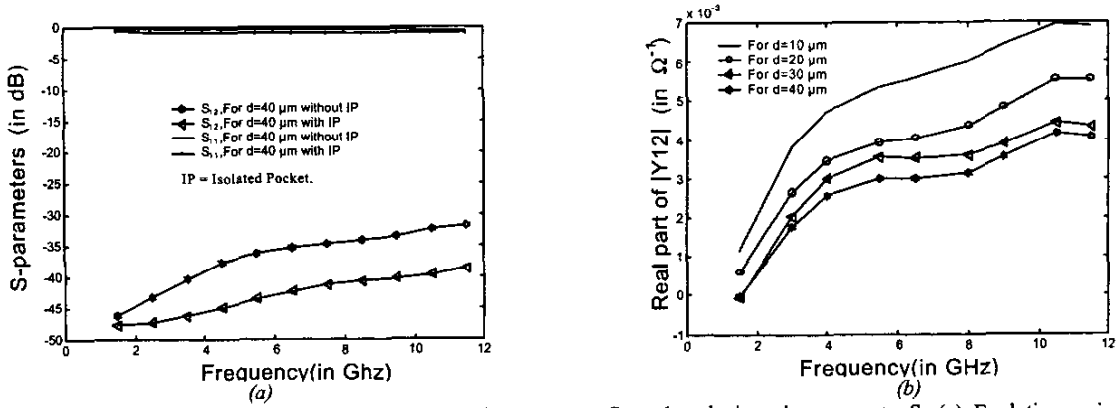

Fig.5 Effects of the isolation pockets on the transmission parameter S_{12} and on the insertion parameter S_{11} (a), Evolution against the frequency of the real part of the admittance Y_{12} for different spacing between pads (b) .

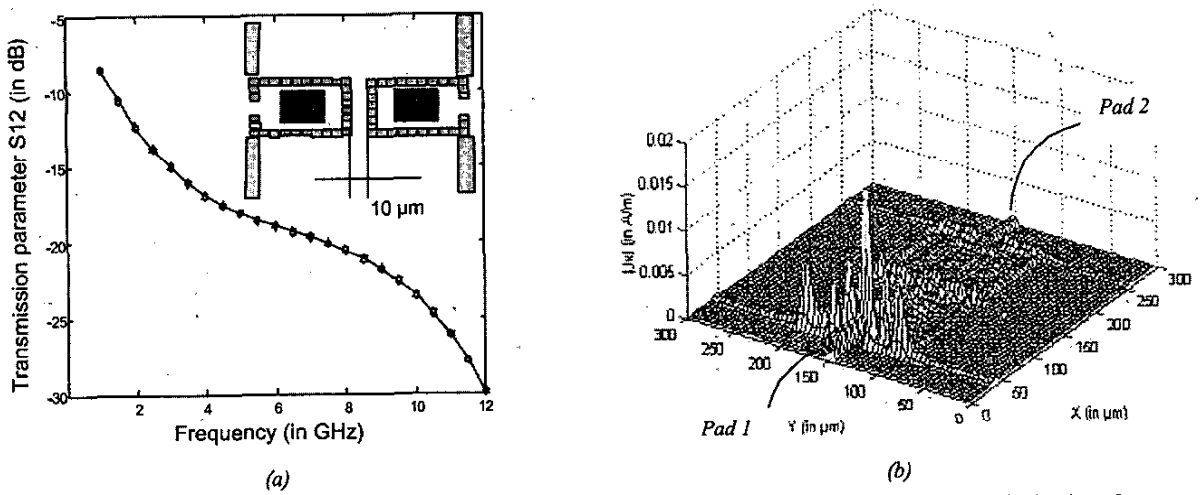

Fig.6 Effects of the two isolation pockets on the transmission parameter S_{12} against the frequency (a) and Distribution of the current density Jx (x,y) (b) at 12 GHz with a 10 µm pad spacing.

Tab.1 Comparison with measurements from [1].

P⁻ Si Substrate Resistivity	Transmission Parameter (in dB) Without Isolated Pocket								Transmission parameter (in dB) With One Isolated Pocket							
	@ 2 GHz		@ 4 GHz		@ 6 GHz		@ 8 GHz		@ 2 GHz		@ 4 GHz		@ 6 GHz		@ 8 GHz	
5-8 Ω-cm	-37.4	*-31.0*	-33.5	*-29.0*	-30.3	*-28.0*	-28.2	*-30.5*	-47.5	*-44.0*	-45.0	*-43.5*	-43.0	*-43.0*	-41.0	*-42.0*
25-50 Ω-cm	-42.5	*-40.0*	-39.0	*-37.0*	-36.4	*-35.0*	-33.3	*-34.0*	-53.3	*-55.5*	-51.1	*-53.0*	-48.2	*-50.0*	-45	*-47.5*

: Measurement from [1] - $d=35\ \mu m$ $w=10\ \mu m$, $\Delta x=100\ \mu m$, $\Delta y=100\ \mu m$, $\Delta p=5\ \mu m$
: Our modeling approach.

In Fig 5-b, the frequency dependence between 2 and 12 GHz of the real part of the Y_{12} parameter, which stands for $1/R_1'$ in [1], is displayed for different values of d, the substrate resistivity being 25 Ω.cm. This dependence confirms the substrate resistivity influence on the deterioration of the isolation performances which are rapidly degraded between 2 and 4 GHz. In Fig 6-a, two guard rings are considered with a 60 µm spacing between pads ; the isolation which has, in that case, to be compared with the results in Fig 5-a, is seen increasing with frequency due to the low spacing between the two guard rings (see Fig 6-a) but ever greater than 35 dB, its minimum value in Fig 5–b. Fig 6-b illustrates the current distribution which appears with comparable intensity in both rings.

Table 1 summarizes the comparison between measurements given in [1] and the above approach. Results of the proposed simulation and the measurements are fairly comparable, discrepency between the two results being around 2 dB except in the lower frequency range. In that case a quasi-static approach can complete the investigation but, it should be notice that in these simulations, 5 µm spacing between via is considered while this data, known to be with little impact on the effects of via fence [6], was not available in reference [1].

IV. CONCLUSIONS

Without resorting to intensive measurements, extricate mixed effects of substrate resistivity, frequency and ground vicinity on isolation capability of circuits in silicon based technology is the task of the EM approach presented here. Interconnects like via are not simulated as isolated elements but included in their actual environment. Introducing the via in the description of the surface rather than in the integral operator provides effective results without inducing any supplementary computation effort. The coupling between vias and the parallel plate mode, here neglected, is assumed to have little influence in such environment, the spacing and the coupling between via being thought more significant.

To reinforce isolation capability by introducing isolation pocket for each pad connection, a special care must be taken towards the spacing between Guard rings that requires to be greater than a certain minimum value for an effective isolation. In regard to the used typical values here considered, this minimum value was greater than 10 µm.

REFERENCES

[1] W. Jin, Y. Eo, J. I. Shim, W. R. Eisenstadt, M. Y. Park " Silicon Substrate Coupling Noise Modeling, Analysis, and Experimental Verification for Mixed Signal Integrated Circuit Design ", ", *IEEE MTT-S 2001*, TH3A-3 pp.1727-1730.

[2] J. Gipprich "A New Via Fence Structure for Crosstalk Reduction in High Density Stripline Packages", *IEEE MTT-S 2001*, TH3A-1 pp.1719-1722.

[3] J.Zheng, Yeon-Chang Hahm,V.K.Tripathi, A.Weisshaar "CAD-Oriented Equivalent-Circuit Modeling of On-Chip Interconnects on Lossy Silicon Substrate", *IEEE Trans. on MTT*, vol.48 pp.445-450, September 2000.

[4] J.Bernal, F.Medina, R.Boix,M.Horno " Fast Full-Wave Analysis of Multistrip Transmission Lines Based on MPIE and Complex Image Theory", *IEEE Trans. on MTT*, vol.48 pp. 445-450, March 2000.

[5] G. E. Ponchak, E. M. Tentzeris, J. Papapolymerou "Coupling Between Microstrip Lines Embedded in Polyimide Layers for 3D-MMICs on Si ", *IEEE MTT-S 2001*, TH3A-2 pp.1723-1726.

[6] R. Abhari, G. V. Eleftheriades, Emilie van Deventer-Perkins " Physics-Based CAD Models for the Analysis of vias in Parallel-Plate Environments ", *IEEE Trans. on MTT*, vol.49 pp.1697-1707, October 2001.

[7] P. Mezzanotte, M. Mongiardo, L. Roselli, R. Sorrentino, W. Heinrich" Analysis of Packaged Microwave Integrated Circuits by FDTD ", *IEEE Trans. on MTT*, vol.42 pp.1796-1800, September 1994.

[8] R. Sorrentino, F. Alessandri, M. Mongiardo, G. Avitabile, L. Roselli " Full-Wave Modeling of Via Hole Grounds in Microstrip by three-Dimensional Mode Matching Technique ", *IEEE Trans. on MTT*, vol.40 pp.2228-2233, December 1992.